Design of third order sigma-delta modulator for bio-medical applications

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Abstract:- Communication is playing a key role in the field of communication engineering since a longtime. As biomedical filed is playing the major role in these days we can make the best use of these. In this paper we will find the best configuration for modulators that meets your needs the desired specifications with dissipation of minimum power. We use third order architecture and single loop topology. The nature of the signal is of low pass that is will allows only low power signals to pass through it. We reduced the values of SNR to make use in bio-medical applications.

Keywords: Analog-to-digital conversion,3rd order sigma detla modulation, Quantizer, Integrator, sampler.

1 INTRODUCTION

In any electronic system, data converter is a major component. Generally the signals are in the form of analog signals. The electronic form of analogue signals may be processed by robust, flexible, and reliable processing of digital signal, as a result the conversion from analog to digital becomes basic. Here we are using a sigma delta modulator through which we can convert digital signals into analog. In the earlier period of pulse width modulation around 1962, the sigma delta modulator was first introduced. In VLSI technology modern converters are often hard to implement. Because these conventional methods in their filters and conversion circuits requires specific analog components and their circuits are very sensitive to noise and interference. Conventional methods use low frequency of sampling, which is usually the signals nyquist rate. These converters makes extensive use of stated below keeping these things in mind, people go over to sampling converters.The sigma delta converters are used because of the following reasons.

1. Increased reliability
2. Additional bandwidth
3. Low power

The sigma delta analog to digital converter is now the key feature of this is the use of many low-cost, high-resolution applications analog to digital converters is that it is based on an oversampling approach which uses a high frequency technique of modulation and removal of the use of anti-aliasing filters in the converter source.

The new trend where the Internet of Things (IOT) alludes to everything that can be associated with the web or atleast to a nearby network In this new concept, low-power and low-cost devices are needed in healthcare, home sensors or smart cities, and where they are similar to electronic play a paramount role. In the electronic industry, the man-week cost is a crucial factor for the overall price of the integrated circuits(ICs)which increases with the complexity of the design of certain circuits .In the context of IOT more than having energy and area efficient circuits is also important to develop circuits that are similar to design in order to decrease the complexity and consequently the man week overhead cost another design issue and according to the international technology road map for semiconductors. In electronic communication, the analog to digital convertor converts the analog signal which is continuous in time and amplitude into the digital signal which is discrete in time and quantized in amplitude. In order to convert analog signals into digital there are many techniques out of which we use sigma delta modulation to get the fast and accurate results. A general analog to digital convertor consists of anti analysing filter which only allows the low power signals, a sampler and a quantizer. The analog signal is passed through the AAF as it passes only low power signals eliminating high power signals. Then that low power signal is sampled in order to get a discrete signal and that discrete signal is passed through the quantizer and gives a digital signal as output.

Generally there are six orders in sigma delta modulation out of which we choose the 3rd order in order to maintain the stability of the system. In case if we use the 1st and 2nd order sigma delta modulation the value of SNR will decrease which results in the decrement of the order of the system. If we use the higher orders then there will not be absence stability in the system. For a 3rd order sigma delta modulator, it is built by cascading three discrete time integrators with each integrator receiving weighted feedback path from digital to analog convertor.

The quantization noise is a model of quantization error introduced by quantization in analog to digital convertor (ADC) in the tele-communication system and also in signal processing. It is rounded error between the analog input voltage to the ADC and the output digitized value, the noise is non-linear and signal dependent.

Depending on the sampling rate the Analog-to-Digital Converter can be divided into two parts, the sigma delta convertor is used for 0 to high resolution power optimizing. For the conversion from analog to digital we have two types of conversion techniques

1. Nyquist convertor
2. Over sampling convertor

Nyquist convertor:

In this type of convertor we have to satisfy either the high frequency or low sampling frequency. On that samples the signal at fN=2*F at nyquist rate, where fN is the sample rate

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and F is the bandwidth of the input signal, the other signal is sampled at a much higher rate. The over sampled sigma delta modulator performs oversampling as

Where K is the ratio of oversampling(OSR) given by

Over-sampling:

It converts the continuous signal into discrete signal. In this we have conversion region in rescuition vs bandwidth plain.

Fs>2fm(Nyquist rate)

Fs>2*(bandwidth)

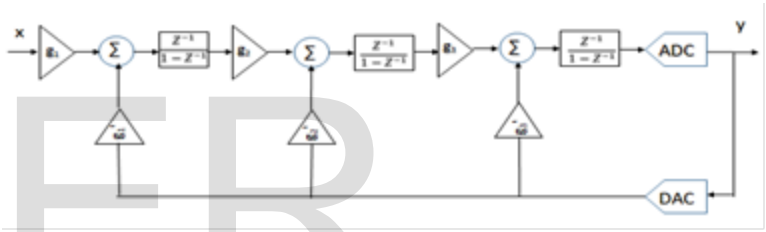
If the value of fs is in between 10 to 512 then fs is said to be oversampled.

Signs are frequently inspected at the required base rate for economy, resulting in the quantization clamor being repeated over the converter's entire pass band. On the off chance that a sign is examined at a rate a lot higher than the Nyquist rate and afterward carefully separated to confine it to the sign data transfer capacity there are the accompanying focal points: computerized channels can have better properties (more keen rolloff, stage) than simple channels, so a more honed enemy of associating channel can be acknowledged and after that the sign can be downsampled giving a superior outcome a 20-piece ADC can be made to go about as a 24-piece ADC with 256× oversampling the sign to-commotion proportion because of quantization clamor will be higher than if the entire accessible band had been utilized. With this method, it is conceivable to get a powerful goals bigger than that gave by the converter alone, the SNR improvement is 3 dB (equal to 0.5 bits) per octave of oversampling not suitable for certain applications. Along these lines, oversampling is normally combined with commotion forming (see sigma-delta modulators).Oversampling is commonly utilized in sound recurrence ADCs where the necessary examining rate (ordinarily 44.1 or 48 kHz) is low contrasted with the clock speed of commonplace transistor circuits (>1 MHz). For this situation, by utilizing the additional data transmission to disseminate quantization mistake on the frequencies of the band, the precision of the ADC can be enormously expanded at no expense. Moreover, as any associated sign are likewise regularly out of band, associating can frequently be totally killed utilizing minimal effort channels.

A sigma-delta ADC first encodes and then applies an analogue signal with high frequency delta sigma modulation to an digital filter to form a high resolution but low sample frequency digital output. Then temporary use of signal with lower resolution simplifies the circuit design and improves the efficiency. For example if we consider the fit band watch that actually shows the heartbeat, steps, time it is actually an analog signal we cannot convert that into digital signal directly so in that case we use the Analog to digital convertor. The analog to digital convertor is generally used in many of the ways such as in software-defined radio(SDR),Digital audio broadcasting(DAB),Digital video broadcasting(DVB),Universal mobile telecommunication system(UTMS),Code division multiple access(CDMS),Global system for mobile communication(GSM),cable modem, ,mobile TV etc.

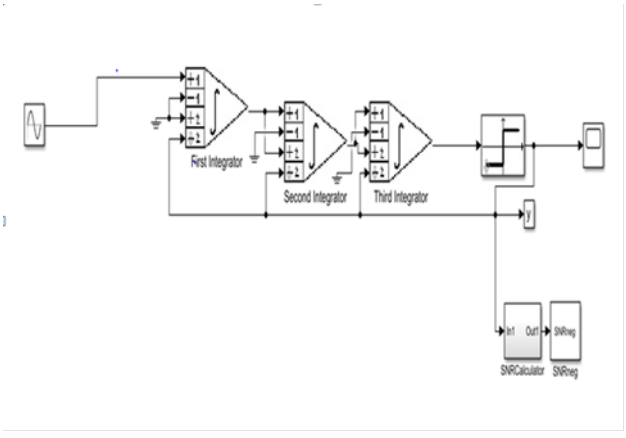
The exhibition of an ADC is fundamentally described by its transfer speed and sign to-commotion proportion (SNR). An analogue to digital Convertor's transmission power is described essentially by its testing rate numerous elements affect an ADC's SNR, including goals, linearity, and precision (how well the quantization levels coordinate the genuine simple sign), association, and jitter. The SNR of an ADC is frequently abridged as far as its viable number of bits (ENOB), the quantity of bits of each measure it returns that are by and large not commotion. A perfect ADC has an ENOB equivalent to its goals. ADCs are picked to coordinate the transfer speed and required SNR of the sign to be digitized. On the off chance that an ADC works at an inspecting rate more noteworthy than double the transfer speed of the sign, at that point per the Nyquist–Shannon testing hypothesis, immaculate remaking is conceivable. The nearness of quantization blunder restricts the SNR of even a perfect ADC. In any case, if the SNR of the ADC surpasses that of the info signal, its belongings might be ignored bringing about a basically ideal computerized portrayal of the simple information signal.

2 Procedure for Paper Submission



3 Result And Discussion

As the over sampling ratio of the feed forward structure increases the signal to noise ratio by DB value increases stability of the system increases since we are using the bio medial applications we prefer the low over sampling ratio so use the sampling frequency of 50 hertz for which we get the SNR by DB value of 94.57 and signal to noise ratio bits value of 15.41.



The output of modulator in the z-domain under linear analysis is equated as

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EQUATION

Kq is the gain of the quantizer

Where stands as integrator scaling

For the first order, noise shaping should be reduced as

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^1 E(z)$$

For the second order, the noise shaping should be reduced as

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^2 E(z)$$

For the third order, the noise shaping should be reduced as

$$Y(z) = z^{-3}X(z) + (1 - z^{-1})^3 E(z)$$

The coefficients of the integrator are fulfilled when

$$k_q a_1 a_2 a_3 = 1$$
$$k_q a_2 a_3 = 3$$
$$k_q a_3 = 3$$
$$k_q = 1$$

therefore the values of a_1, a_2, a_3 are

$$k_q a_1 = 1/3$$
$$k_q a_2 = 1$$
$$k_q a_3 = 3$$
$$k_q = 1$$

4. Behavioral simulation in simsides:

SIMSIDES is the sigma delta Simulator based on SIMULINK. It is designed as a tool box for the sigma delta modulator in MATLAB-SIMULINK environment. It can be used to model any sigma delta modulator structure implemented with either continuous time or discrete time-circuit techniques. All the basic building blocks libraries are built for simulation using SIMSIDES. IT is made up of all the sigma-delta modulator building blocks such as integrator, comparator, quantizer, etc. The behavioral models of these building blocks consider the most critical error mechanism of different circuit techniques. Despite being very functional the implementation of the behavioral models of each basic building blocks requires several sets of elementary SIMULINK blocks. Calculating the histograms and output spectra using the functions given by MATLAB toolbox. Certain analyzers are carried out using a series of SIMSIDES specifies functions such as signal to noise ratio, harmonic etc.

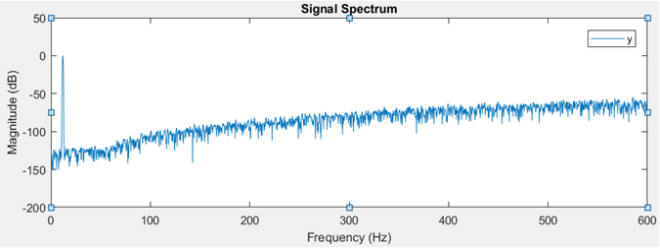
The following are the model parameters including circuit level non-idealities

Building Blocks	Variables	Values
First Integrator	C int 1	24e-12
	Innoise1	0
	Cs11	6e-12
	Cs12	6e-12
	a01	2.5+03
	gm1	10e-03
	io1	5.0e-03
	ron1	60
	Cnl1	0
	avnl1	0
	Cpar1	0.6e-12
	Cload	2.28e-12
Second and third Integrator	C int 2	3e-12
	Innoise2	0
	Cs12	1.5e-12
	Cs22	1.5e-12
	a02	2.5+03
	gm2	10e-03
	io2	5.0e-03
	ron2	650
	cnl2	25e-6
	avnl2	15e-2
	avnl3	0
	avnl4	0
Input Parameters	Fs	5.12e6
	Fi	5e3
	Ts	1/fs
	M	130
	N	65536
	Ain	0.5
	temp	175
	osp	2.7

RESULT:

Node spectrum analysis:

The graph given below shows the input analog signal converted into digital signal and since it is an analog to digital signal converter it consists of noise in this graph we have shown that the signals separated from the noise using the feed



Comparision of values at different OSR values:

Oversampling ratio	SNR by DB
50	85.6690
65	93.9416

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100	106.1350
112	106.1350
128	107

Conclusion:

A sigma delta analog to digital converter is programmed to connect system components. Op-amp, one of the most powerful essential components with an open loop frequency of 96decibals and a gain bandwidth of 57MHZ, allows the control system circuits to work smoothly. It is also used as a summing circuit that helps to provide the integrator with the input of the differential feedback. Accompanied by a comparator with high speed a latched style comparator is used to compare the input signals with a reference signal and provide the corresponding result that is then fed to the system feedback path to 1 bit digital to analog circuit. This process is iterated and output of the system achieves a pulse of the digital signal. In order to minimize static power diffusion, the sigma delta analog to digital converter was designed to simulate using a standard 0.9 cadence tool. Dynamic latch comparator was designed to minimize the dissipation of static power.

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